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Also the domain of scientific, numerical computing is covered. The material in the book is based on the author contributions presented at the 3rd International Workshop on Algorithms and Parallel VLSI Architectures, held in Leuven, August 29-31, 1994.

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DIGITAL SIGNAL PROCESSING (DSP) APPLICA- tions often require computing speeds that cannot be achieved by standard signal processor implementations. In this case the use of customized dataflow processors is necessary to meet the

High-speed parallel Viterbi decoding: algorithm and VLSI

IEEE TRANSACTIONS ON ACOUSTICS. SPEECH. AND SIGNAL PROCESSING. VOL. 38, NO. 1 .
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The purpose of this chapter is to present an algorithm for the computation of the eigenvalue decomposition (EVD) by a Jacobi-type method, which can be mapped to an efficient, parallel very-large-scale integration (VLSI) architecture.

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Integration | Algorithms and parallel VLSI architectures

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Parallel VLSI CAD Algorithms

two-phase $\hat{1}/4$ oding algorithm because there is still no need to store the variable node messages in the multi-layered algorithm. In this paper, we propose a multi-layer parallel decoding algorithm and VLSI architecture for high throughput LDPC decoding. The data con $\hat{1}/4$ licts between layers are resolved by modifying the LLR update rules.

Multi-Layer Parallel Decoding Algorithm and VLSI

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