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Predicting the Phase Noise and Jitter of PLL-Based Frequency Synthesizers Introduction 4 of 52 The Designer's Guide Community [www.designers-guide.org](http://www.designers-guide.org) also rules out any PLL that is implemented with a phase detector that has a dead zone.

### **Predicting the Phase Noise and Jitter of PLL-Based**

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### **Designer - Wikipedia**

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## **Graphic Designers : Occupational Outlook Handbook: : U.S**

SLVA157 4 Choosing Inductors and Capacitors for DC/DC Converters Figure 5. TPS62204 (1.6V) Efficiency vs Load Current vs Input Voltage With 4.7- $\mu$ H Wire-Wound Inductor,  $R_{dc} = 240 \text{ m}\Omega$  / ISAT = 700 mA Output Capacitor The designer can downsize the output capacitor to save money and board space.

## **Choosing Inductors and Capacitors for DC/DC Converters**

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